Low-loss Power Semiconductors

Background and Objective

Further electrification and the use of low-carbon power sources are essential from the viewpoints of the conservation of the global environment and the highly efficient use of energy. The wider use of low-loss and downsized next generation power converters has become an important common technological task faced by electrification promotion technologies associated with plug-in hybrid cars, electric vehicles, IH equipment and heat pump equipment. This task is also faced by power stability control technologies for the maximum utilisation of nuclear and renewable energies. For this reason, great expectations are placed on the practical use of SiC power semiconductors which can achieve a lower power loss, higher voltage and downsizing compared to Si semiconductors which are used for conventional power conversion equipment.

This project theme is introduced to develop a low defect single SiC crystal production technology and improving the performance of high voltage devices with a view to developing practical systems using low-loss and downsized power converters.

Main results

1. Clarification of the behaviour of crystallographic defects in SiC crystal growth

The formation of crystallographic defects (dislocations and stacking faults) in the growth process of a single crystal layer (epitaxial layer) and device fabrication process was studied in detail using a synchrotron topography and transmission electron microscopy for the purpose producing a SiC epitaxial layer with a low defect density. The study clarified the propagation of dislocations from the SiC substrate to the epitaxial layer during the growth process and the generation mechanism of dislocations and stacking faults at the interface of the substrate and epitaxial layer (Fig. 1)[1] as well as in the device fabrication process (Fig. 2)[2].

2. Reduction of dislocations in SiC crystal growth

It is known that when basal plane dislocation (dislocation on the (0001) plane) exists in a SiC epitaxial layer, the reliability of a high voltage device (bipolar type) declines. Through the high resolution analysis of crystallographic defects, it has been established that the growth of an epitaxial layer on a SiC substrate with a relatively small off-angle (inclination angle of 4° from the (0001) plane) can achieve a higher quality as the basal plane dislocations reaching the substrate surface are almost completely converted to a different type of dislocations (Fig. 3)[1].

3. Reduction of point defects in a SiC crystal

The $Z_{1/2}$ type point defects in a SiC epitaxial layer reduce the carrier lifetime while increasing the power transport loss of a high voltage device. The application of the $Z_{1/2}$ point defect elimination method (interstitial carbon diffusion method) developed by the CRIEPI to a thick SiC epitaxial layer has lengthened the carrier lifetime to more than 20 microseconds which is approximately eight times longer than the normal lifetime (Fig. 4)[3].

References

1) Phys. Status Solidi B, 246, 1553 (2009)/Chapter 3 in “Silicon Carbide”, Wiley-VCH (2009)
2) Materials Science Forum, 615, 477 (2009), ibid, 645, 323 (2010)
3) Materials Science Forum, 645, 77 (2010)

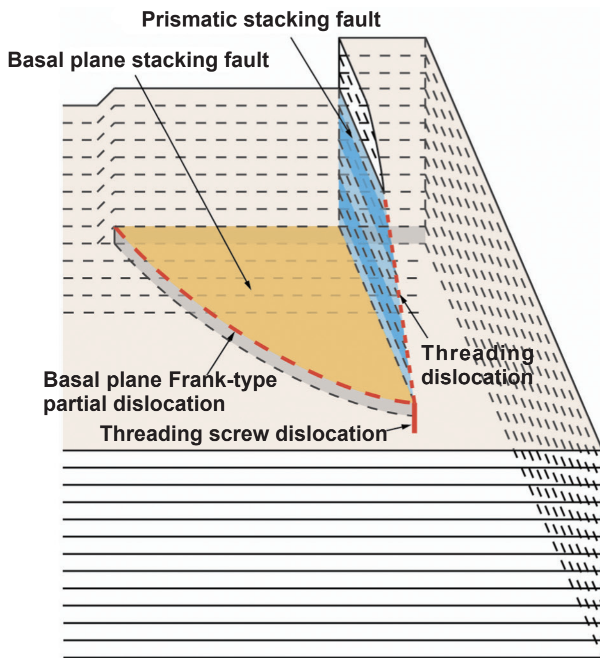

Fig. 1 Formation model of stacking faults (carrot-type defects) during epitaxial growth

An original model is proposed to illustrate the conversion of threading screw dislocation in a substrate to a different type of defect accompanying the stacking fault (carrot-type defect: compound defects of the basal plane stacking fault and prismatic stacking fault) during epitaxial growth.

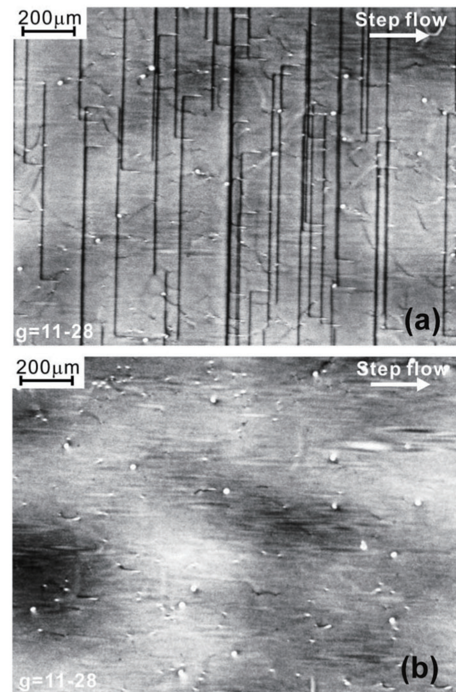

Fig. 2 Synchrotron X-ray topography image of SiC epitaxial layer after heat treatment (use of (a) conventional crucible and (b) improved crucible)

It has now been established that interfacial dislocation (shown as contrasting black lines on Image (a)), which is generated in the heat treatment of a SiC crystal during the device fabrication process, originates from thermal stress at the time of heat treatment. The use of an improved crucible where the temperature distribution is more uniform can suppress the generation of this type of interface dislocation (b).

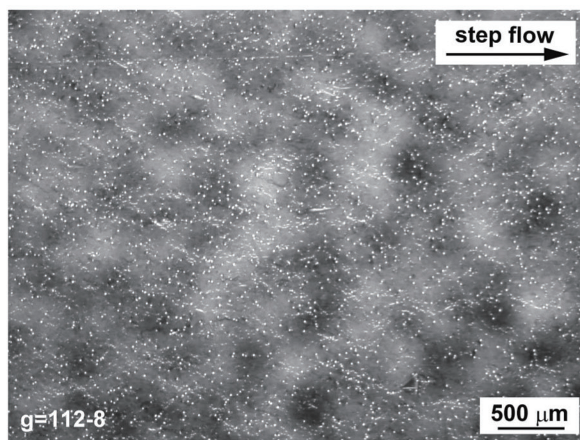

Fig. 3 Synchrotron X-ray topography image of SiC epitaxial layer which has no basal plane dislocation

A SiC epitaxial layer with no basal plane dislocation (no dislocation shown as contrasting black lines) has been successfully developed. This has been achieved by increasing the probability of the conversion of the dislocation structure in the propagation process of dislocation from the substrate to an epitaxial layer. This increase is the result of the epitaxial growth of a SiC epitaxial layer on a SiC substrate with an inclination angle of 4° to the (0001) plane.

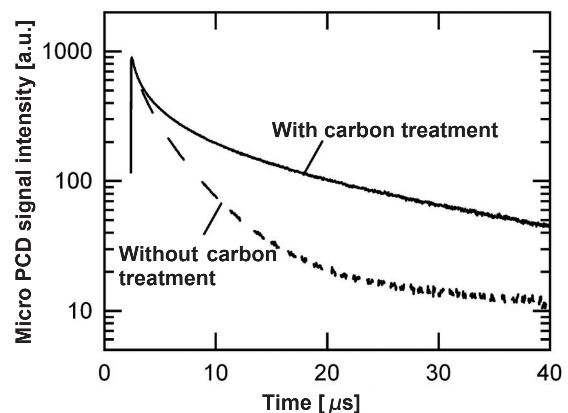

Fig. 4 Analysis results for the carrier lifetime of a SiC epitaxial layer (decay curve of micro-PCD signal)

The carrier lifetime of a 250 μm thick SiC epitaxial layer is substantially lengthened through the application of the interstitial carbon diffusion method (carbon-ion implantation and heat treatment) to the epitaxial layer. (The decay time of the micro PCD signal, which indicates the carrier lifetime, has lengthened from 3.3 μs before treatment to 27 μs after treatment.)